AMENDMENTS TO THE SPECIFICATION

Please amend the specification as indicated below, in order to correct minor errors contained therein.

Please amend the paragraph on page 19, lines 14-25, as follows:

In the sustain periods SUS1 to SUS5, sustain pulses according to a value weighed to each of the subfields SF1 to SF5 are outputted to the sustain electrodes 13 and the scan electrodes 12. For example, in the subfield SF1, the sustain pulse is applied to the sustain electrodes 13 once, the sustain pulse is applied to the scan electrodes 12 once, so that the discharge cell or cells 14 selected in the write period [[P2]] AD1 perform the sustain discharge twice. Furthermore, in the subfield SF2, the sustain pulse is applied to the sustain electrodes 13 twice, the sustain pulse is applied to the scan electrodes 12 twice, so that the discharge cell or cells 14 selected in the write period [[P2]] AD2 perform the sustain discharge four times.

Please amend the paragraph on page 20, lines 1-12, as follows:

As described above, in the respective subfields SF1 to SF5, the sustain pulses are applied to the sustain electrodes 13 and the scan electrodes 12, once, twice, 4 times, 8 times and 16 times, respectively, so that the discharge cell or cells emit light at brightness (luminance) according to the number of pulses. Namely, the sustain periods SUS1 to SUS5 are periods when the discharge cells selected in the write periods AD1 to AD5 discharge at the number of times according to the weighed amount of brightness. Furthermore, in the sustain periods SUS1 to SUS5, the phase of shift clock SCK provided to the clock phase adjuster 9 of Fig. 1 is adjusted. The adjustment of the phase of the shift clock SCK will be described later in detail.

Please amend the paragraph on page 29, lines 10-17, as follows:

Here, a case where the latch failure occurs in the flip-flop circuit 131 is considered. As shown in Fig. 7(b), the test pattern TPb comes to keep a high or low portion in successive two clock periods 2T or more without being inverted in one clock period T due to the latch failure in the flip-flop circuit 131. This also causes the test pattern TPc to keep a high or low portion in successive two clock periods 2T or more without being inverted in one clock period T.

Please replace the Abstract with the new Abstract appearing on the following page.